AMENDMENTS TO THE CLAIMS

Claims 1-8 (Cancelled)

9. (Currently Amended) A semiconductor memory device comprising:

a memory cell array formed of a plurality of memory cells arranged in rows and columns, and each provided with first and second transistors having gate electrodes and impurity regions forming sources/drains as well as one capacitor, bit lines corresponding to said plurality of columns and word lines corresponding to said plurality of rows; and

a sense amplifier connected to said bit lines and used for amplifying a signal for normal access to said memory cells and refresh, wherein

said first transistor is arranged as a transistor for normal access to be used for the normal access and not to be used for the refresh access, ~~and~~

said second transistor is arranged as a transistor for refresh to be used for the refresh access and not to be used for the normal access, and

said semiconductor memory device employs a background refresh system for automatically refreshing said memory cell regardless of presence and absence of a refresh signal when said access sense amplifier is operating.

10. (Original) The semiconductor memory device according to claim 9, wherein

said bit lines are formed of an access bit line and a refresh bit line, said first transistor is connected to said access bit line, and said second transistor is connected to said refresh bit line.

11. (Currently Amended) The semiconductor memory device according to claim 9, wherein

said word lines are formed of an access word line and a refresh word line, said sense ~~amplifiers include~~ amplifier comprising an access sense amplifier to be activated via said access word line and a refresh sense amplifier to be activated via said refresh word line, and said access sense amplifier and said refresh sense amplifier operate independently of each other.

Claim 12 (Cancelled)

13. (Currently Amended) A semiconductor memory device comprising:

a memory cell array formed of a plurality of memory cells arranged in rows and columns, and each provided with first and second transistors having gate electrodes and impurity regions forming sources/drains as well as one capacitor, bit lines corresponding to said plurality of columns and word lines corresponding to said plurality of rows; ~~and~~

switching control means for eliminating a complementary relationship between said memory cell and said complementary memory cell, establishing an equivalent relationship between said memory cell and said complementary memory cell, and operating both the memory cells equivalently, and

a sense amplifier connected to said bit lines and used for amplifying a signal for access to said memory cells and refresh, wherein

said memory cells are paired with complementary memory cells, respectively, and said sense amplifiers are formed of a normal sense amplifier connected to said bit line coupled to said

memory cell and a complementary sense amplifier connected to a complementary bit line coupled to said complementary memory cell.

14. (Original) The semiconductor memory device according to claim 13, wherein said word lines are formed of a first word line connected to said memory cell and a second word line connected to said complementary memory cell.

15. (Original) The semiconductor memory device according to claim 14, wherein at least one of said first and second word lines is activated to activate at least one of said sense amplifier and said complementary sense amplifier.

16. (Original) The semiconductor memory device according to claim 13, wherein one of the transistors in said memory cell is arranged as a transistor for normal access, the other transistor is arranged as a transistor for refresh, one of the transistors in said complementary memory cell is arranged as a transistor for normal access, and the other in said complementary memory cell is arranged as a transistor for refresh.

17. (Original) The semiconductor memory device according to claim 16, wherein said bit lines are formed of an access bit line and a refresh bit line, said word lines are formed of an access word line and a refresh word line, said sense amplifiers are formed of an access sense amplifier and a refresh sense amplifier, said normal access transistor in the memory cell is connected to said access bit line, said refresh transistor in the memory cell is connected to said refresh bit line, said normal access transistor in the complementary memory cell is

connected to said complementary access bit line, and said refresh transistor in the complementary memory cell is connected to said complementary refresh bit line.

Claim 18 (Cancelled)

19. (Currently Amended) The semiconductor memory device according to claim [[18]] 13, wherein

said switching control means includes sense amplifier connection control means for eliminating said complementary relationship by changing the state of connection of said sense amplifier only to said normal bit line to the state of connection to said normal and complementary bit lines, and changing the state of connection of said complementary sense amplifier only to said complementary bit line to the state of connection to said access bit line and said complementary access bit line different from said normal bit line and said complementary bit line.

20. (Currently Amended) A semiconductor memory device comprising:

a memory array provided with memory cells arranged in rows and columns, and each including at least one transistor having a gate electrode and impurity regions forming source/drain as well as one capacitor, bit lines corresponding to the plurality of columns and word lines corresponding to the plurality of rows:

a cell plate forming one of electrodes of said capacitor and using said impurity region as an opposite electrode; and

cell plate potential changing means for changing the potential on the cell plate,

wherein said cell plate potential changing means is time-varying potential changing means for correcting the potential on said cell plate varying with time due to leak of potentials in said capacitor.

21. (Original) The semiconductor memory device according to claim 20, wherein said cell plate is arranged for each of said word lines.

22. (Original) The semiconductor memory device according to claim 21, wherein said cell plate has a belt-like form extending along said word line, and said memory array is positioned along said belt-like cell plate.

Claim 23 (Cancelled)

24. (Currently Amended) The semiconductor memory device according to claim [[23]] 20, wherein

said cell plate potential changing means can reset an amount of change effected on said cell plate when accessing the memory cell.

25. (Currently Amended) The semiconductor memory device according to claim [[23]] 20, wherein

said cell plate potential changing means changes the potential on said cell plate by flowing a current through said capacitor.